Amendments to the Specification:

Please amend the specification as follows:

Please replace the paragraph starting at Page 1/Line 16 with the following rewritten paragraph:

An SRAM of the related art is described with reference to Fig. 1. Fig. 1 shows a circuit structure of a unit cell (hereinafter referred to as an SRAM cell) of the related art SRAM by which a **[[cash]]** **cache** memory is structured. In a case where a word line signal WL lies a low voltage potential, forming two CMOS (Complementary Metal Oxide Semiconductor) inverters in loop connection enables data to be stably stored. That is, one of the CMOS inverts has an input formed of a data storage node V1 to allow inverted data of data stored in the node V1 to be output to a data storage node V2 and the other of the CMOS inverts has an input formed of a data storage node V2 to allow inverted data of data stored in the node V2 to be output to the data storage node V1.

Please replace paragraph starting at Page 34/Line 22 with the following rewritten paragraph:

The NMOS transistors N4, N5 and N2 are disposed in the left-side P well region and the PMOS transistors P1, P2 are disposed in the central N well region while the NMOS transistors N1, N3 are disposed in the right-side P well region. In Fig. 26B, wiring related to the data storage nodes V1 **[[ad]]** **and** V2 forming wiring inside the cell are completed inside the cell and designated by solid lines, with resulting junctions being designated in black circles.

Please replace paragraph starting at Page 40/Line 2 with the following rewritten paragraph:

The drive transistor N1 ha a source connected to the ground potential GND and a read word line signal RWL is output from drains of the transistors P1, N1. Moreover, the inverter has an ~~input~~ **output** to which the drain of the NMOS transistor N2 is connected and the NMOS transistor N2 has a source connected to the ground potential GND and a gate to which the inverted read block selection RPB is input **(as shown in Fig. 51)**. With this circuit structure, the two-input NOR circuit is comprised of three transistors, whereby a read word line signal RWL is selected when the inverted word line signal WLB and the inverted read block selection signal RPB take the low voltage potential.